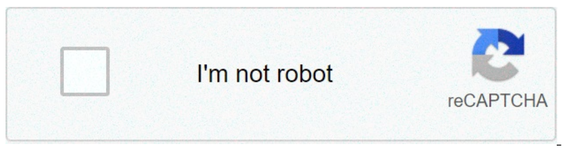

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The 8086 microprocessor is one of the families of 8086,80286,80386,80486, Pentium, Pentium I, II, III Ã ¢ â,¬ |. Even the X86 family. The X86 is a 16-bit microprocessor chip designed by Intel "between the early 1976, ie destined to be used as the CPU on computers, 16 bits means its interior designed to work with 16-bit binary words with words 16-bit binary. Microprocessor 8086 chips is a topic Ã ¢ for B.Tech (3-year) students of ã, electronics and computer science. These notes provide information about the 8086 chip that plays an important role. These notes are designed Specially in PDF format for an easy download and contain handwritten notes in simple and simple languages with complete diagrams of architecture and its complete explanation. The notes covers the following topics in detail: - 8086 Family overview: - Architecture, diagram of block of 8086, details of the sub-committees as EU, Biu; Memory segmentation and physical address calculations, the transfer program, addressing modes, instruction formats, PIN schema and description The different signals.Instruction set of 8086: instructions execution times, assembler instructions format, data transfer instructions, arithmetic instructions, jumping instructions, loop operations, NOP and HLT instructions, flag manipulation instructions, logical instructions, Moving instructions and rotate instructions, directives and operators, programming examples .download for more queries related to Notes Comment Comment below ... | !!!! We will solve it as soon as possible. Intel 8086A Intel C8086 rare processor Microprocessor In Intel C8086 in Purple Ceramic Dive Package with the Brazed Side Pinsgeneral InformationLaunched1978Discontinued1998 [1] Common Producer (s) of Intel, AMD, NEC, Fujitsu, Harris (Intersil), Oki, Siemens, Texas Instruments, Mitsubishi, Panasonic (Matsushita) PerformanceMax. CPU CLOCK RATE5Ã ¢ MHz 10 MHZDATA Width 16 BitsAddress Width20 BitSarchitecture and ClassificationIn.ã, Feature Â »Size 33.SexSstructionSÂ® SETX86-16-16CYSICAL SPECIFICATIONSTRANSISTORS29 million-processarel 8087, Intel 8089Package (s) 40 Pins Dipset (s) Dip40Products , Models, VariantsVaricialLintell 8085Succetrestor50186 and 80286 (both of which were introduced in the first months of 1982) 8086 [2] (also called iaPX 86) [3] is a 16-bit microprocessor designed by Intel between the first months of 1976 and 8 June 1978, when it was released. Intel 8088, released on 1 July 1979, [4] is a slightly modified chip with an external 8-bit data bus (allowing the use of more economic and less supported ICS), [note 1] and Ã It is remarkable as the processor used in the original IBM PC design. The 8086 gave rise to the X86 architecture, which eventually became a successful line of intel. On 5 June 2018, Intel released a limited edition CPU to celebrate the 40th anniversary of Intel 8086, called the Intel Core i7-8086K processor. [4] Story context in 1972 Intel launched 8008, the first 8-bit microprocessor. [Note 2] A set of instructions creating Datapoint Corporation with programmable CRT terminals in mind, which turned out to be generic enough is implemented. The necessary device several additional uses to produce a functional computer, partly due to it that is packaged in a small 18-pin "Memory package", which excluded the use of a separate address bus (Intel was first of all a Manufacturer DRAM AL moment). Two years later, Intel launched 8080, [Note 3] which uses the new 40-pin DIL packages originally developed for Calculator ICS to enable a separate address bus. It has an extensive set of instructions that is source-compatible (not compatible at the binary level) with the 8008 [5] and also includes some instructions at 16 To make programming easier. The 8080 device has eventually been replaced by the 8085 load-load (1977), which is sufficient with a single power supply + 5 V instead of the three different operating voltages of previous chips. [Note 4] Other well-known 8-bit microprocessors that emerged during these years are Motorola 6800 (1974), general tool Pic16x (1975), Mos Mos 6502 (1975), Zilog Z80 (1976), and Motorola 6809 (1978). The Intel 8086 CPU image processor The first project X86 8086 project has begun in May 1976 and was originally understood as a temporary substitute for the ambitious and delayed IAPX 432 projects. It was an attempt to attract the attention of the less delayed to 16 and 32 bits the processors of other producers (such as Motorola, Zilog, and National Semiconductor) and at the same time to counter the threat of Zilog Z80 (designed by former intel employees), which became a great success. Both architecture and physical chip were therefore developed rather quickly from a small group of people, and using the same base microarchitecture elements and physical realization techniques as used for the slightly older 8085 (and for which 8086 also It would work as a continuation). Marketed as a compatible source, [6] 8086 was designed to allow language assembly for 8008 [necessary quotation], 8080, 8085 or to automatically convert into equivalent (not optimal) 8086 source code, with little or no manual drawing. The programming and education model set is (vaguely) based on the 8080 in order to make this possible. However, the 8086 project has been expanded to fully support 16-bit processing. The new types of instructions have been added as well; Full support for integers with sign, base + addressing offset, and self-repetition operations were similar to Design Z80 [7], but they all realized a little more general in 8086. Directly nested support instructions Languages Algol - Family, like Pascal and PL / M have also been added. According to the main architect Stephen P. Morse, this was the result of a more software-centric approach than in the design of previous intel processors (designers had work experience with compiler implementations). Other improvements including microprogram multiply and instructions divide and a bus structure more suited to future cover (eg 8087 and 8089) and multiprocessor systems. The first revision of the instruction set and high-level was ready after about three months, [Note 5] and, as no CAD tools were not used, four engineers and 12 bis of the people layout were simultaneously working on the chip. [Note 6] The 8086 took a little more than two years from the idea to the work product, which was considered rather fast for a complex project in 1976th 1978. The 8086 was sequenced [Note 7] using one Mixture of random logic [8] and MicroCodice and was implemented using NMOS loading circuitry with approximately 20,000, active transistors (29,000 counting all Roma and PLA sites). It was soon to move to a new NMOS refined production process called HMOS (high performance MOS) that intel originally developed for the production of static fast RAM products. [Note 8] This was followed by HMos-II, the HMO-III versions, and, finally, a completely static CMOS version for battery powered devices, made with Chmos Intel processes. [Note 9] The original chip measured 33a mmâ² and minimum size was 3.2a ÃžÃ¼m. The architecture was defined by Stephen P. Morse with some help from Bruce Ravenel (the architect of 8087) in final revision refining. Logic Designer Jim McKevitt and John Bayliss were the lead engineers of the hardware level development team [note 10] and Bill Pohlman the project manager. The inheritance of 8086 is lasting in the instruction set of the personal computer and server instructions; The 8086 also lent his last two figures for extensively extended versions of design, such as Intel 286 and Intel 386, all that eventually became known as the X86 family. (Another reference is that the PCI ID supplier for devices Is 8086h.) Details 8086 Assigning min and max bus and operation mode all internal logs, as well as internal and external data buses, are 16th bits wide, which firmly established the "16-bit microprocessor" identity of 8086. A 20 bit external address bus provides a 1â, MB (220 (220 (220 1048.576). This address space is routed through the internal memory "Segmentation". The data bus is multiplexed with the address bus to fit all control lines in an in-line package 40-pin standard. It provides a 16-bit address bus I / O, supporting 64K separate I / O space. The maximum linear address space is limited to 64 KB, © simply because the internal address / index registers are only 16 bits wide. The programming beyond the 64K memory limits involves the adjustment of the segment registers (see below); This difficulty existed until the 80386 architecture has introduced more extensive registers (32-bit) (the hardware of the memory management nell'80286 did not help in this sense, since © its registers are still only 16 bits wide). Mode Some of the hardware control pins, which carry signals essential for all external operations, have more than one function depending on whether the device is operated in a minimum mode. The previous mode is destined to small single-processor systems, while the latter is for medium or large systems that use more than one processor (a type of multiprocessor mode). The maximum mode is required when using a coprocessor 8087 or 8089. The voltage on PIN 33 (MN / MX) determines the mode. The modification of changing the function of some other pins of PIN state 33, the majority of which has to do with the way in which the CPU manages the bus (local). [Note 11] The mode is typically wired in the circuit and therefore can not be changed by the software. The work of these modes are described in terms of timing diagrams in Datashes Intel datasheets and manuals. In minimum mode, all the control signals are generated from the same 8086. Registers Registers instructions and Intel 8086 19 18 17 16 15 15 14 13 12 11 10 09 08 07 06 06 04 03 03 01 06 05 04 03 02 01 00 (BIT POSITION) main Recorders Ã Ah to Ax (primary battery) Ã BH BL BX (BASE, accumulator) Ã CH CL C CX (counter, accumulator) Ã DH DL DX (accumulator, Extended ACC) indices registers registers 0 0 0 0 0 SI index Source 0 0 0 0 0 0 Destination Index 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 SC 0 0 0 0 0 IP ISTRISSIONE POINTER sEGMENT SEGMENTORSS CS 0 0 0 0 0 DS segment code 0 0 0 0 0 segment data 0 0 0 0 0 extra segment SS 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0- C BANGELLI the 8086 has eight 16-bit registers more or less general (including the stack pointer but the pointer of excluding 'instruction, the flags register and the segment registers). Four of them, AX, BX, CX, DX, can also be accessed as twice the number of 8-bit registers (see figure) while the other four, one, of, bp, sp, are only 16-bit. Due to a compact encoding inspired by the 8-bit processors, most of the instructions have an operation for an address or two addresses, which means that the result is stored in one of the operands. At most one of the operands can be in memory, but this memory operand can also be the target, while the other operand, the source can be recorded or immediate. A single memory location can also be used as a source and destination, among other factors, further contributes to the code density comparable to (and often better than) eight-bit machines at the time. The degree of generality of most of the records is much greater than all'8080 or nell'8085. However, 8086 records were more skilled than most of his contemporaries minicomputers and implicitly are also used by some instructions. While it is perfectly reasonable for the programmer assembly, this makes the register allocation for the more complicated compilers compared to other 16-bit orthogonal processors and 32 bits of the time as the PDP-11, VAX, 68000, etc. On the other hand, be more smooth than 8-bit Microprocessers rather minimalist but ubiquitous as the 6502, 6800, 6809, 8085, MCS-48, 8051 and other machines based on contemporary accumulators, is significantly easier to build a code generator Efficient for architecture 8086. Another factor for this is that the 8086 also introduced some new instructions instructions present in 8080 and 8085) to better support based on high-level programming languages stack as Pascal and PL / M; some of the most useful instructions are mem-op push and ret size, supporting the "Pascal calling convention" directly. (Many others, like PUSHA IMMed and enter, were added in subsequent processors 80186, 80286 and 80386). A 64a KB (one segment) growing stack more toward lower addresses is supported in hardware; 16-bit words are inserted into the stack, and the upper part of the stack is pointed to by SS: SP. There are 256th interrupt, which can be invoked by both hardware and software. The interrupts can cascade, using the stack to store the return addresses. The 8086 has 64a K 8-bit (or alternatively 32a of K 16-bit word) space I / O port Flags The 8086 has a register of 16-bit flags. Nine of these flags are active condition code, and indicate the status of processor current: Carry flag (CF), Parity flag (PF), carry auxiliary flag (AF), flag zero (ZF), flag sign (SF), flag Trap (TF), interrupt flag (IF), direction flag (DF), and the overflow flag (OF). also referred to as the status word, the layout of the flags register is as follows: [9] Bit 15-12 11 10 9 8 7 6 5 4 3 2 1 0 Flag Ã OF TF DF IF SF ZF AF Ã Ã Ã PF CF segmentation see also: x86 segmentation memory there are also four 16-bit segment registers (see figure) that allow the CPU 8086 to access one megabyte of memory in an anomalous way. Instead of concatenation register segment with the address register, as in most of the processors whose address space exceeds their log size, the 8086 moves the 16-bit segment only four pieces left before adding it to 16-bit Offset (16A + offset segment) , thereby producing a 20-bit external address (or effective or physical) from the 32-bit segment: offset pair. As a result, each external address can be defined by 212 = 4096 different segments: Offset pairs. Ã 0110 1000 1000 1000 0000 0111Ã Segment, 16-bit, shifted 4 bits to the left (or multiplied by 0x10) + aa 0011 0100 1010 1001 Offset, 16 bits Ã 0110 1011 1101 0001 1001 Address, 20 bits Although considered complicated and cumbersome by many programmers, this system also has advantages; a small program (less than 64A KB) can be loaded from a fixed offset (eg 0000) in its own segment, avoiding the need to transfer, with more to 15th bytes of waste alignment. Compilers for 8086 family support two types of commonly pointer from near and far. Near pointers are offsets to 16-bit implicit code or associated with the segment of the program data and therefore can be used only in parts of a program small enough to fit in a segment. Far pointers are 32-bit segment: offset pairs to resolve a 20-bit external address. Some compilers also support huge pointers, which are as far pointers except that pointer arithmetic on a huge pointer comes as a 20-bit linear pointer while the pointer arithmetic on a far pointer wraps in its offset without touch the part of the segment to 16-bit address. To avoid the need to specify "memory models" near and far on numerous pointers, data structures and functions, compilers also support that specify default pointer size. The tiny (64k max), small (128K max), compact (data> 64K), medium (code> 64 K), large (code, data> 64 K), and huge (individual arrays> 64K) models covering practical combinations of proximity, by far, and huge pointers for code and data. The small model means that the code and data are shared in a single sector, as well as in most of the 8-based processors And they can be used to build .com file for example. Precompilated libraries are often available in different versions compiled for different memory models. According to Morse et al., [10]. The designers actually contemplated using an 8-bit turn (instead of 4-bit), in order to create a 16Ã, MB physical address space. However, since this would have forced segments to start on the boundaries of 256 bytes, and 1ã, MB was considered very large for a one around 1976, the idea has been rejected. In addition, there were not enough available on a pin for the other four address bus pins package 40-pin low cost. In principle, the space of the x86 series address could be extended in subsequent processor by increasing the displacement value, Purcha © applications obtained their segments by the operating system and do not make assumptions about the equivalence of different segments :. couples Offset [Note 12] in practice the use of pointers "large" and similar mechanisms had spread and the dish made possible 32-bit addressing with offset registers 32 â â bits in 80386 randomly extended limited addressing range so more generally (see below). Intel would have decided to implement in memory words of 16 bits (which would have eliminated the BHE signal (Bus High Enable) with much of the complexity already described address bus). This means that all the object codes of instructions and data should be read in 16-bit units. The users of 8080 realized a long time ago, in hindsight, that the processor makes very efficient use of its memory. From a large number of 8-bit object codes, the 8080 produces compact object code as some of the most powerful minicomputer on the market at the moment. [11] If the 8086 can store 8-bit object codes and thus the efficient use of the memory 8080, then it can not guarantee that (16-bit) operating codes and data will lie on a boundary address even-odd bytes. The first 8-bit opcode will shift the 8-bit next instruction byte in an odd or instruction to 16 bits to an even-odd-byte boundary. By implementing the BHE signal and the additional logic necessary, the 8086 allows instructions to exist as 1 byte, 3-byte characters or other object codes odd bytes. [11] In short, it's a trade off. If the memory addressing is simplified so that the memory is accessible only in 16-bit units, memory is used less efficiently. Intel has decided to make more complicated logic, but the use of more efficient memory. This was at a time when the memory size was considerably smaller, and at a premium, of what users are used to today. [11] The more software porting old programs could ignore small segmentation and just use plain 16-bit addressing. This allows the 8-bit software to be quite easily brought to 8086. The authors of most DOS implementations have taken advantage of this by providing an application programming interface very similar to CP / M and partecipates © including the simple .com format executable file, identical CP / M. This was important when the 8086 and MS-DOS was new, because © has allowed many existing CP / M applications (and others) to be quickly made available, greatly easing the acceptance of new platform. Code Example The following source code assembler 8086/8088 is a subroutine named _memcpy that copies a byte block of data of a given size from one position to another. The data block is copied to a byte at a time, and the data movement and the loop logic uses 16-bit operations. 0000 1000 0000 1000 0000 1000 55 0000 1001 89 E5 0000 1003 06 0000 1004 8B 4E 06 0000 1007 E3 11 0000: 1009 8B 76 04 0000: 100C 8B 7E 02 0000: 100F 1E 0000 1010 07 0000: 1011 8A 04 0000 : 1013 88 05 0000 1015 46 0000: 47 1016 0000 1017 49 0000 1018 0000 75 F7: 07 0000 101A: 101B 5D 0000: 101C 29 C0 0000: 101E C3 0000: 101F; _memcpy (DST, src, len); Copy a block of memory from one location to another. ; ; Stack parameters entrance; [BP + 6] = len, number of bytes to copy; [BP + 4] = src, address of the source data block; [BP + 2] = daylight saving time, address of the target data block; ; return registers; AX = zero org 1000h; Start 0000: 1000h _memcpy proc BP; Set the BP MOV call frame, ES SP push; Save es MOV CX, [BP + 6]; Set cx = made len jcxz; If Len = 0, Return Mov Yes, [BP + 4]; SI = SRC MOV of, [BP + 2]; Set of = DST DS push; Set es = ds pop es cycle MOV al, [yes]; Upload to from [SRC] MOV [of], to; Store at a [Summer time] Inc Yes; Increase SRC INC; December CX DST increase; Decrease Len Jnz cycle; Repeat the es pop loops; restore es es es BP; Restore Previous Call Sub Ax Frame, Ax; Set AX = 0 RET; End Return Proc The previous code uses BP (base pointer) register to establish a call frame, a stack area that contains all the parameters and local variables for the execution of the subroutine. This type of caller convention supports the residential and recursive code and has been used by most algol-like languages from the end of the 1950s. The above routine is a rather cumbersome way to copy data blocks. The 8086 provides dedicated instructions for copying byte strings. These instructions support that the source data is stored on DS: Yes, the destination data is stored on ES: and that the number of items to be copied is stored in CX. The aforementioned routine requires the source and the destination block to be in the same segment, then DS is copied e.g. The above ring section can be replaced by: 0000: 1011 FC 0000: 1012 F3 0000: 1013 A4 CLD; Copy to a higher address radius repeater; Repeat up to cx = 0 movsb; Move the data block This copy the data block a byte at a time. The REP statement repeats the following MovsB until CX is zero, automatically increasing and decreasing CX as you repeat. Alternatively, the MOVSW statement can be used to copy 16-bit words (double bytes) at a time (in which CX CX counts the number of words copied instead of the number of bytes). Most assemblers recognize the EDUCATION REPLY correctly if used as an online prefix on the MOVSB statement, as in REP MOVSB. This routine will work correctly if interrupted, since the program counter will continue to point to the REP instruction until the block copy is completed. The copy will then continue from where it was interrupted when the interrupt service routine returns control. Simplified block diagram on the performance on Intel 8088 (a variant of 8086); 1 = main records and index; 2 = segment records and IP; 3 = Adder address; 4 = internal address bus; 5 = instruction queue; 6 = control unit (very simplified!); 7 = bus interface; 8 = internal data; 9 = ALU; 10/11 / 12 = External address / data / control bus. Although partially shaded by other design choices in this particular chip, the multiplexed address and data buses lightly limit performance; 16-bit or 8-bit quantity transfers are performed in a four-clock access cycle, which is faster than 16 bits, although more slow on 8-bit quantities, compared to many 8-bit contemporary CPUs. Because the instructions vary from one to six bytes, recovery and execution are performed simultnulous and decoupled in separate units (as it remains in today's X86 processors): the bus interface unit feeds the flow of instructions to the execution unit Through a 6-byte prefetch queue (a form of freely coupled pipe), accelerating the operations on registers and immediate, while memory operations have become lens (four years later, this performance problem has been set with 80186 and 80286). However, the complete architecture (instead of the partial) 16-bit with a complete width is intended that the 16-bit arithmetic instructions could now be performed with a single ALU cycle (instead of two, through internal transport, as in the 8080 and 8085), greatly accelerating these instructions. Combined with orthogonations of operations against types of operand and addressing modes, as well as other improvements, this has made the performance gain compared to 8080 or 8085 enough significant, despite the cases where previous chips could be faster (see below). Execution times for typical instructions (in cycles of [12] Register-Registered Instructions Register Instant Log Registry-Memory Memory-Register Memory-immediate MOV 2 4 8 + EA 9 + EA 10 + EA ALU 3 4 9 + EA, 16 + EA, 17 + EA JUMP REGISTER Ã ¢ Â € ¥ 11Ã ¢; Label Ã ¢ â € ¥ 15Ã ¢; Condition, Label Ã ¢ â € ¥ 16 Integer Multiply 70 ~ 160 (depending on the working data and size) Included and included Divide 80 ~ 190 (depending on the data of the operand and size) Included any EA EA = TIME To calculate an effective address, ranging from 5 to 12 cycles. The times are better, better, On the prefetch state, alignment of instructions and other factors. As you can see from these tables, the operations on registers and immediate were fast (between 2 and 4 cycles), while the instructions and jumps of memory operand were rather slow; The jumps took more cycles than on the simple 8080 and 8085, and 8088 (used in the IBM PC) was also hindered by his narrowest bus. The reasons why most of the instructions related to the memory were lens have been three times: freely coupled recovery and execution units are efficient for prefetched education, but not for jumps and access to random data (without Special measures). No added calculation of the dedicated address was offered; Microcodice routines have had to use the main aluminum for this (although there was a dedicated segment + offset compendium). The address and data buses have been multiplexed, forcing a slightly longer bus cycle (33 ~ 50%) compared to the typical 8-bit contemporary processors. However, memory access services have been drastically improved with the next generation of Intel of 8086 familiar CPUs. 80186 and 80286 were both the hardware to calculate dedicated addresses, saving many cycles and 80286 also had a separate address (not multiplexed) and data buses. Floating point The 8086/8088 could be connected to a mathematical coprocessor to add floating hardware / microdote performance. Intel 8087 was the standard mathematical coprocessor for 8086 and 8088, which operates on 80-bit numbers. Manufacturers such as Cyrix (compatible with compatible) and Weitek (not compatible) (not 8087 compatible) eventually invented high-performance floating shorts that competed with 8087 versions. The clock frequency was originally limited to 5 MHz, [Note 13] But the latest versions in HMOS were specified for 10 MHz. HMMO-III and CMOS versions were produced for a long time (at least a little in the 90s) for embedded systems, even if his successor , the 80186/80188 (which includes some peripherals on chip), has been more popular for built-in use. The 80c86, the CMOS version of the 8086, was used in the GridPad, Toshiba T1200, HP 110, and finally the 1998 lunar sensors of 1998. For the packaging, the Intel 8086 was available in both ceramic and ceramic packs of plastic. A ceramic variant D8086 Plastic variant P8086 Intel 8086 variant list Model number Frequency technology Temperature technology Temperature range Release price date (USD) [List2 1] 8086 5Ã, MHz [13] HMOS 0 Â ° C to 70 Â ° C [14] 8 June 8, 1978 [15] $ 86.65 [16] 8086-1 10 MHz HMOS II COMMERCIAL 8086-2 8Ã, MHZ [13] HMOS II COMMERCIAL JANUARY / FEBRUARY 1980 [17] $ 200 [17] [18] 8086-4 4ã, MHz [13] Hmos Commercial $ 72.50 [List2 2] [19] I8086 5ã, MHz Hmos Industriale Ã ¢ '40 Ã ¢ Â ° C A + 85 Â ° C [14] May / June 1980 [14] $ 173.25 [14] M8086 5Ã, MHZ HMMO MILITARY GRADE Ã, '55 Ã, Â ° C A + 125 Â ° C [20] 80C86 [21] CMOS ^ IN QUANTITY OF 100. ^ Reduced price of 21% from USD $ 99.00, no information in the value of the quantity listed. Derivatives â €

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